A Low Power Class-AB Audio Power Amplifier With Dynamic Transconductance Compensation in 55 nm CMOS Process

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***Abstract*—This paper presents a Class-AB audio power amplifier with state-of-the-art power efficiency and performance. In this work, the second stage transconductance of the three-stage power amplifier can be dynamically compensated, in order to automatically adjust the amplifier pole according to the operating condition of the output stage. Working with a current sensing module, the proposed dynamic transconductance compensation scheme is more power-efficient to allocate the frequency of non-dominant-pole under a specified stability requirement. A prototype chip is designed and fabricated using 55 nm CMOS process. The measured static current consumption of the core circuit is 0.35 mA with a 1.8 V supply voltage. −85 dB THD+N, 106 dB signal dynamic range and 55 mW output power are verified in silicon under a wide range of load capacitance from 5 pF to 20 nF. Measurement result shows the proposed transconductance compensation technique is effective in both constant voltage supply mode and dynamic supply (Class-G) mode.**

***Index Terms*—Audio power amplifier, class-AB, CMOS integrated circuit, low power.**

I. Introduction

NOWADAYS, high performance headphone power amplifier (PA) gains rapidly increased applications in high-end products like high-fidelity audio players and mobile phones. The main specifications of an audio power amplifier include: maximum output power, total harmonic distortion + noise (THD+N), dynamic range, static power consumption, click-pop noise, power supply rejection ratio (PSRR), offset, chip area, etc. [1]. Since most of these specifications are correlated, higher specifications, like THD+N or DR, would then penalize the power consumption. An optimal way to design the PA is to make good trade-off based on its target application [2].

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In some low-end products, two-stage amplifier with a moderate DC open-loop gain is adopted, which is easy to be kept stable even under large load variations, while with inferior harmonic distortion [3]. For better closed-loop linearity, three-stage Class-AB mode amplifier topology has gained more attention in the past decade for its higher gain and better power efficiency with the capability to handle a wide range of capacitive load [4]. Although frequency compensation technique of damping-factor-control was proposed [5], conventional Class-AB driver is not an optimal solution for a signal with large real-time amplitude variation. Because the transconductance (g_m) of the output stage significantly changes as a function of the output current amplitude, the relative frequency space between the gain-bandwidth (GBW) and the non-dominant-pole could vary. As a result, to guarantee the closed-loop stability of the amplifier, it is over-designed for the worst phase margin scenario, which burns more than necessary power during normal operation. To address this over-compensation issue, reference [6] introduced a low power Class-AB/B hybrid PA scheme at the cost of design complexity and chip area for the Class-B integration. Voltage level shifters were used to enable the Class-B driver if the signal became larger than a threshold voltage. To further improve the power efficiency, current sensing technique was introduced into headphone drivers [7]. For a small output signal, a conventional Class-AB driver was adopted. As the output signal increased, the proposed PA could gradually turn on the auxiliary Class-B driver, by monitoring the output current using a g_m replica circuit. Inductor current sensing technique was also widely adopted in Class-D headphone drivers but mainly for the speaker protection purpose [8]–[10].

In this paper, an audio power amplifier designed in 55 nm CMOS process is presented, which is embedded as a key building block in a system-on-chip (SOC). A power-efficient frequency compensation scheme for the Class-AB driver is proposed with a dynamic transconductance adjustment circuit. With an dedicated output current sensing module, the current-to-voltage control signals can dynamically adjust the MOS resistors inside the second stage of the main amplifier and thus optimize the pole location. Compared with a conventional Class-AB, the proposed scheme can reduce the power waste for frequency over-compensation when given a specified stability requirement. The proposed transconductance compensation scheme is verified in both constant voltage supply mode and dynamic supply (Class-G) mode.

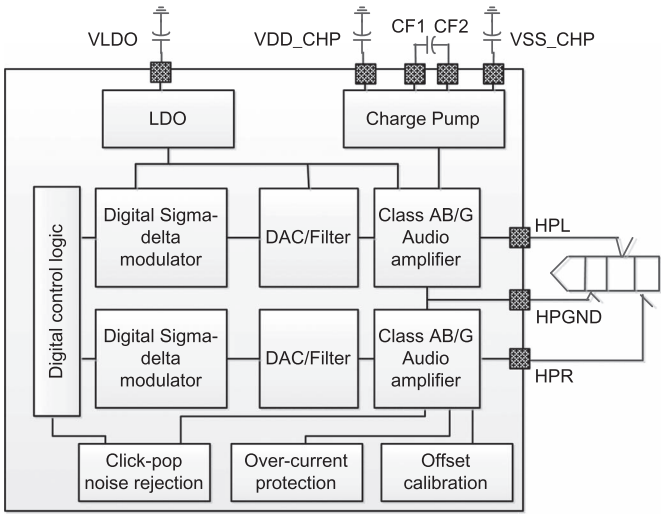


Fig. 1. Top architecture of the proposed audio power amplifier chip.

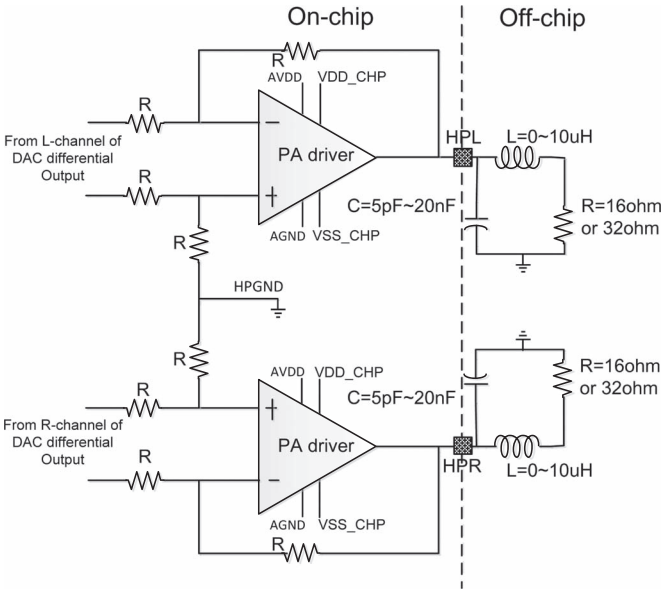


Fig. 2. Zoom-in structure of the power amplifier block.

This paper is organized as follows. In Section II, the power amplifier circuit is analyzed. Section III presents the circuit implementation. Section IV demonstrates the experimental result, followed by the conclusion in Section V.

II. Proposed Integrated Stereo Power Amplifier Topology

Fig. 1 shows the top architecture of the proposed audio power amplifier. The input digital signal is modulated by the digital sigma-delta modulator and thus, most of the quantization noise is shaped into the high frequency band. The input digital signal is converted into the analog signal in the audio frequency band of 20 KHz and is processed by a following analog filter. The audio signal in its analog form is then amplified by the Class-AB power amplifier. A single-flying capacitor charge pump generates both positive and negative supply voltages for the output driver stage [11]. This dedicated power supply can isolate the internal noise-sensitive circuits from the output power supply noise. The first two stages of the power amplifier use 1.8 V analog supply and ground while the third Class-AB stage operates with +/−1.8 V power supply generated from the charge pump. In Class-G mode, if the input signal amplitude is large, the charge pump provides +/−1.8 V for the power amplifier, otherwise +/−0.9 V are generated. The supply voltage can be switched smoothly to prevent any obvious crossover distortion [7]. The click pop noise suppression circuit can attenuate the click pop noise during power on and off. The offset calibration circuit dynamically measures the output offset voltage and then adjust the DC bias.

Fig. 2 shows the zoom-in structure of the power amplifier block, including both right and left sound channels with two differential-to-single-ended amplifiers. From the perspective of different application scenarios, the proposed driver can tolerate various load conditions ranging from 5 pF to 20 nF, 0 H to 10 μH, 16 ohm or 32 ohm, as required in consumer electronics [12].

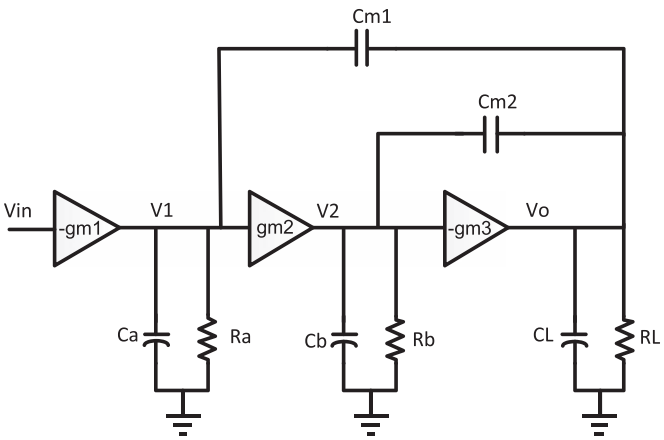


Fig. 3. A standard three-stage amplifier with Nested Miller compensation.

III. Power Amplifier Circuit Scheme

A. Three-Stage Amplifier

Fig. 3 shows the simplified model of a standard three-stage amplifier with Nested-Miller-Compensation (NMC) [13]. Assuming the transconductance of each stage is g_{mi}, the local RC parameter of each stage is R_aC_a, R_bC_b, R_LC_L and the Miller compensation capacitors are C_{m1} and C_{m2}, respectively. The open-loop gain A_0 as well as dominant/non-dominant poles $p_1 \sim p_3$ of the whole amplifier can be approximated as (1)–(3) [14], [15]

$$A_0 = g_{m1}g_{m2}g_{m3}R_aR_bR_L \tag{1}$$

$$p_1 \approx \frac{1}{g_{m2}g_{m3}R_aR_bR_LC_{m1}} \tag{2}$$

$$p_{2,3} \approx \frac{g_{m3}-g_{m2}}{2C_L} \pm j\frac{g_{m3}-g_{m2}}{2C_L}. \tag{3}$$

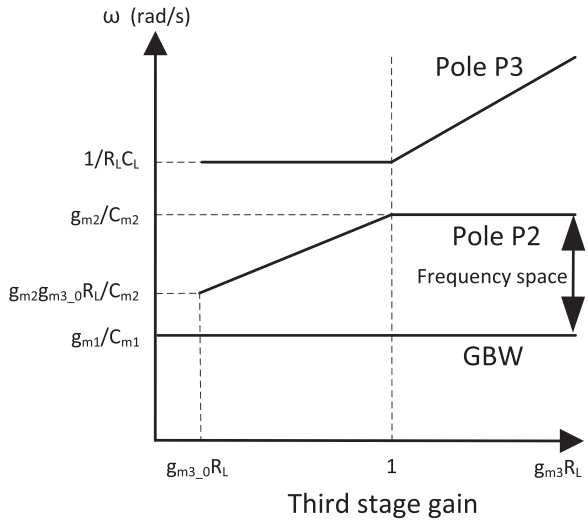


Fig. 4. Typical relationship between GBW, poles and the third stage gain.

The poles from Miller effect need keep stable [16]. Since the output load resistance could be lower to 16 ohm, Class-AB is required for low static power design. Along with the large variation of the third stage transconductance g_{m3}, the output stage gain is also changed as a function of the output current amplitude. Variable g_{m3} implies that the Miller effect pole location is unfixed. With a large output drive current, $g_{m3}R_L \gg 1$ thus, $p_2 = g_{m2}/C_{m2}$ and $p_3 = g_{m3}/C_L$ [15]. On the contrary, for a small static current, $g_{m3}R_L \ll 1$, p_2 and p_3 can be approximately expressed as

$$p_2 = \frac{g_{m2}g_{m3}R_L}{C_{m2}} \tag{4}$$

$$p_3 = \frac{1}{(R_L C_L)}. \tag{5}$$

Defined by the product of the DC-gain and the dominant pole frequency, the gain-bandwidth (GBW) product (the same as unit-gain-frequency for a single pole system) of the three-stage amplifier exhibits a constant value, as expressed in (6). The frequency locations of p_2 and p_3 as a function of the third stage gain $g_{m3}R_L$ can be illustrated in Fig. 4. When $g_{m3}R_L < 1$, p_2 follows g_{m3} from a tiny value of $g_{m2}g_{m3\_0}R_L/C_{m2}$ to g_{m2}/C_{m2}, where g_{m3_0} is the transconductance of the output stage with a nil load current amplitude. Different from p_2, p_3 is almost fixed until $g_{m3}R_L > 1$ and then it begins to move to the high frequency. The minimum frequency of p_2 happens at g_{m3_0}, as derived in (7) where W_{17}, W_{19}, L_{17}, L_{19} are the width and length for transistor M_{17} and M_{19} in Fig. 9

$$\text{GBW} = A_0 \times p_1 = \frac{g_{m1}}{C_{m1}} \tag{6}$$

$$p_2 = \frac{g_{m2}g_{m3\_0}R_L}{C_{m2}} = g_{m2}\sqrt{\frac{2I_s}{C_{ox}}}\left(\sqrt{\frac{W_{17}}{\mu_p L_{17}}} + \sqrt{\frac{W_{19}}{\mu_n L_{19}}}\right)\frac{R_L}{C_{m2}}. \tag{7}$$

B. Proposed Dynamic Transconductance Compensation

The principle of frequency compensation in a multi-stage amplifier is to split the GBW and non-dominant poles by Miller effect until their relative frequency space is large enough to provide a specified phase margin. Shown in Fig. 4, the frequency space must fulfill the phase margin specification at the worst condition of g_{m3_0}. As a result, the frequency space is over-designed for a larger g_{m3}, implying that power saving can be achieved by optimizing g_{m2} correspondingly after monitoring g_{m3}.

A dynamic transconductance compensation (or modulation) technique is proposed to balance the frequency space between the gain-bandwidth and non-dominant-pole as a function of g_{m3}. To better describe the proposed scheme, a normalized transconductance adjustment factor A is introduced, where it can be seen as a function of the third stage transconductance g_{m3}. When $g_{m3}R_L \ll 1$, A is designed to be much larger than that when $g_{m3}R_L > 1$, as shown in Fig. 5(a). Assisted by the adjustment factor A, the frequency space can be increased for a small g_{m3} and decreased for a large g_{m3}, as illustrated in Fig. 5(b). Compared to Class-AB power amplifiers with the conventional Miller compensation method, p_2 in this design exhibits less frequency variation and therefore less power consumption is wasted for over-compensation in the large output current situation.

C. Amplifier Circuit Implementation

Fig. 6 shows the simplified transistor-level schematic of the proposed Class-AB driver. It consists of a telescopic input stage, a current-mode folded second stage, a push-pull Class-AB output stage and a dynamic transconductance compensation function with a current sensing block. The sensed output current amplitude (or g_{m3} of the third stage) is used to generate the control signals VRESN1 and VRESN2 to adjust the variable resistors R_1 and R_2, which are implemented with M_{21} and M_{22}, respectively. VRESP is a fine control signal to tune the transconductance $g_{mM_{24}}$ of M_{24}. Two moscaps M_{23} and M_{25} are used for low frequency signal blockage. Inside the second stage, transistors $M_{26} \sim M_{29}$ are used as a translinear loop floating control to guarantee the stability of the output stage at different process corners. M_{14} and M_{15} are used for gain boosting assisted with the auxiliary amplifier A_u [17]. Fig. 7 shows the schematic of the N-type folded-cascode auxiliary amplifier to regulate M_{14} while a PMOS-input-pair version is adopted for M_{15}. Both Ahuja [18] and Miller compensation techniques are adopted in the proposed driver in order to save power as well as chip area for large capacitive loads. The Ahuja/Miller hybrid scheme is also helpful to extend the amplifier bandwidth at the cost of more complicated compensation circuit [19]. Cascode transistors M_{18} and M_{20} are used in the third stage to improve the output impedance.

The first and second stages of the amplifier utilize 1.8 V power supply from the same LDO. The first stage ground is a clean analog 0 V. The negative power supply of the second and third stages and the positive power of the third stage are supplied from a dedicated charge pump module. By such a power planning, the whole system enjoys a better noise isolation and

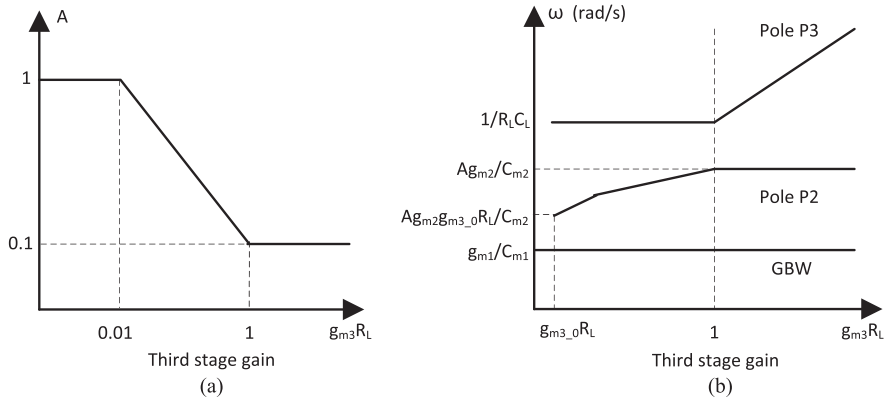


Fig. 5. (a) Proposed relationship between adjustment factor A and the third stage gain; (b) proposed relationship between GBW, poles and the third stage gain.

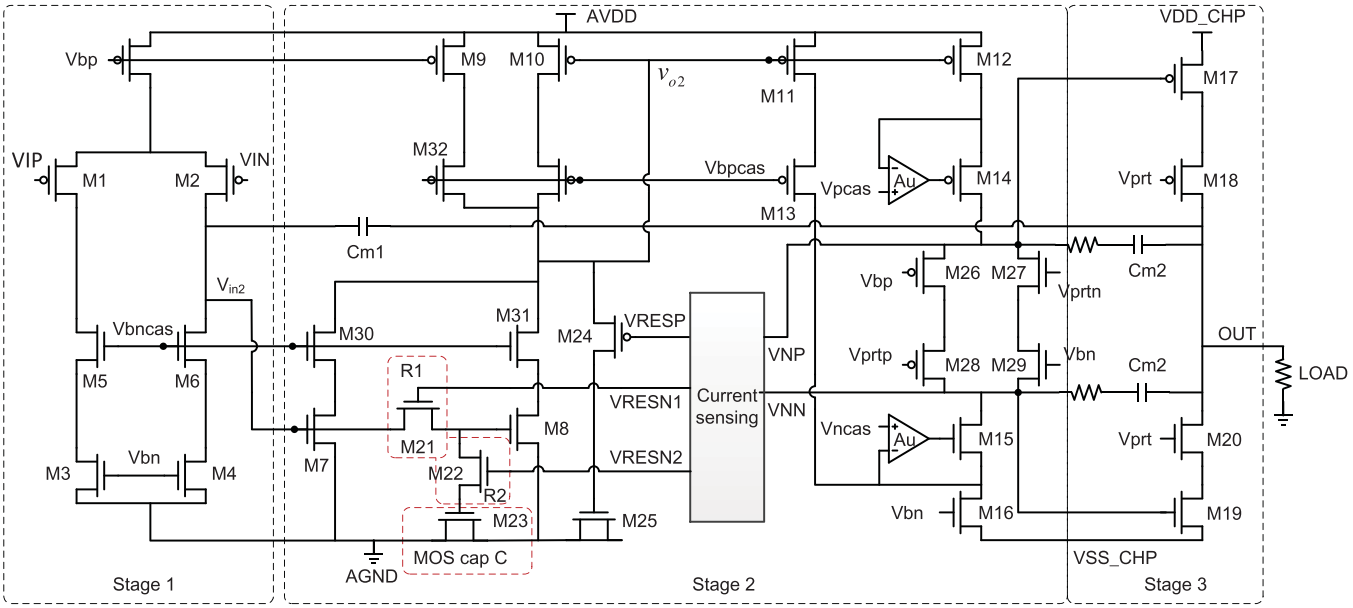


Fig. 6. Proposed Class-AB driver schematic.

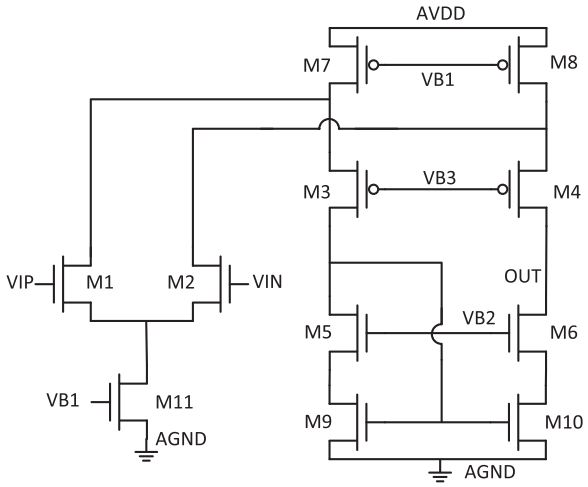


Fig. 7. The schematic of the N-type auxiliary amplifier for cascode PMOS transistor regulation.

the input referred noise is attenuated by the high open-loop gain. By adding the cascode structure with proper bias voltages (Vncas, Vbcas, Vprt, Vbpcas, Vbncas, etc), unsafe transistor operation points are avoided [17]. At the worst case, this three-stage amplifier has a simulated open-loop gain of 102 dB with 6 MHz unit gain frequency and 70° phase margin. The feedback factor is designed to offer a closed-loop gain tuning range from −6 dB to 6 dB.

Fig. 8 shows the simplified small signal model of the proposed dynamic transconductance compensation function of the second stage, where i and r are small signal symbols of the current and equivalent resistor, respectively. As a result, i_{M10} flowing through M_{10} can be expressed as (8), (9)

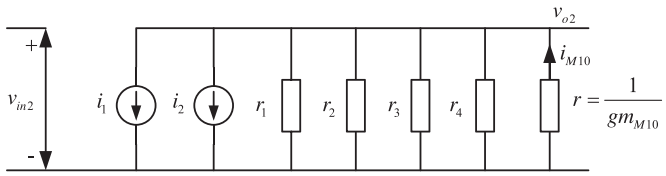
$$i_{M10} = i_1 + i_2 + \frac{v_{o2}}{r_1} + \frac{v_{o2}}{r_2} + \frac{v_{o2}}{r_3} + \frac{v_{o2}}{r_{M24}} \tag{8}$$

$$v_{o2} = \frac{-i_{M10}}{g_{mM10}} \tag{9}$$

$$i_{M10} \approx i_1 + i_2 - \frac{i_{M10}}{r_{M24} g_{mM10}} \tag{10}$$

$$i_1 = \frac{g_{m2}}{10} v_{\text{in2}} \tag{11}$$

$$i_2 = \frac{9 g_{m2} R_2 v_{\text{in2}}}{10(R_1 + R_2)}. \tag{12}$$



$i_1 = gm_{M7} v_{in2}$ $gm_{M7} = \frac{gm_2}{10}$	$r_1 = gm_{M30} r_{M30} r_{M7}$ (ignorable)	$r_3 = gm_{M32} r_{M32} r_{M9}$ (ignorable)
$i_2 = gm_{M8} \frac{R_2 v_{in2}}{R_1 + R_2}$ $gm_{M8} = \frac{9 gm_2}{10}$	$r_2 = gm_{M31} r_{M31} r_{M8}$ (ignorable)	$r_4 = r_{M24}$

Fig. 8. Small signal model of the proposed dynamic transconductance compensation function in the second stage of the amplifier.

Assuming $r_1 \sim r_3$ are much larger than r_4, by combining (10)–(12), i_{M10} can be expressed as (13), where g_{m2} is defined as the conventional second stage transconductance without using the proposed dynamic transconductance compensation function. After the equation rearrangement in (14), the second stage transconductance adjustment factor A becomes a function of R_1 and R_2, which can automatically follow the output stage operation condition:

$$i_{M10} = \frac{g_{m2} v_{\text{in2}} R_1 + 10 g_{m2} v_{\text{in2}} R_2}{10\left(1 + \frac{1}{r_{M24} g_{m\,M10}}\right)(R_1 + R_2)} \tag{13}$$

$$i_{M10} = A g_{m2} v_{\text{in2}}$$

$$\Rightarrow A = \frac{R_1 + 10 R_2}{10\left(1 + \frac{1}{r_{M24} g_{m\,M10}}\right)(R_1 + R_2)}. \tag{14}$$

When the output current has a small amplitude, $r_{M24} g_{m\,M10} \gg 1$ and $R_1 \ll R_2$ thus, $A \approx 1$. On the contrary, for a large output current, $R_1 \gg R_2$ and A can be approximated as

$$A_{\_Io} \approx \frac{1}{10\left(1 + \frac{gm_{M24}}{gm_{M10}}\right)} \tag{15}$$

The schematic of the proposed current sensing circuit used in Fig. 6 is shown in Fig. 9. The output currents of Class-AB driver transistors M_1 and M_2 are mirrored and added as a control signal I_{sense} as expressed in (16), where transistors have the same channel length and I_3 is used to adjust the offset of I_{sense}. For a large output current instantaneous amplitude (> 10 uA), I_3 can be ignored. For nil output (< 100 nA), I_3 makes sure transistors of the current sensing circuit operating in the saturation region. Process, voltage and temperature (PVT) variations can be tolerated by specified phase margin of the amplifier

$$I_{\text{sense}} = |I_{M1}| \frac{W_5 W_7}{W_1 W_6} + |I_{M2}| \frac{W_{10}}{W_2} + I_3. \tag{16}$$

Voltage VRESN1 and VRESN2 automatically follow the sensed output current. According to the simulation, for $I_1 = 0.5$ μA, M_{17} and M_{23} in Fig. 9 set VRESN1 $= 1.2$ V and VRESN2 $= 0.6$ V. As a result, in Fig. 6 MOS resistor $M_{21} \gg M_{22}$. When the sensed current becomes larger than the specified critical high value $I_1 = 10$ μA, the control voltages are VRESN1 $= 0.75$ V and VRESN2 $= 1$ V. At this condition, M_{21} in Fig. 6 enters into the cutoff region. As current I_1 continuously increased, since M_{21} is already cutoff, it cannot further contribute transconductance adjustment. Because all of the internal nodes in the current sensor circuit exhibit low impedances, the response time of this control loop is less than 50 ns, which can be ignored.

It should be noted that, the DC current consumption in the proposed design remains the same in different output conditions. But in order to achieve the same DC-gain, bandwidth and stability requirement, a conventional design with fixed equivalent second stage transconductance must consume more power. The power saving in the proposed circuit can be achieved at the large value of $g_{m3} R_L$ (right region of Fig. 5(b)) by reducing the adjustment factor A. As shown in (3), the dominant pole p_1 is reversely proportional to $g_{m2} g_{m3}$. Therefore, the open-loop -3 dB bandwidth drops for a large g_{m3}, while the phase margin (or stability) degrades for a small g_{m3}. To move the non-dominant pole p_2 to higher frequency for a small g_{m3}, g_{m2} should be a large value which is comparable for both the conventional and proposed designs. The difference is that, in the conventional design, g_{m2} is a constant value, however, in the proposed design, when the instantaneous load current amplitude becomes large, the equivalent g_{m2} is only 10% of that in the conventional design. As a result, p_1 in the conventional design could be much smaller due to a larger $g_{m2} g_{m3}$. In order to increase p_1 (or bandwidth), R_a or R_b or C_{m1} must be reduced, as shown by (3). If R_a or R_b is set to a small value by utilizing short channel length transistors (smaller λ), the DC-gain lose must be compensated with extra current consumption by increasing g_{m1} or other parameters. If C_{m1} is sized with a small value, although the DC-gain is not affected, g_{m1} must be reduced in order to keep the same GBW, which also implies sacrificing the DC-gain. In our proposed design, the DC-gain is not affected by the dynamic transconductance adjustment due to the existence of DC blockage MOS capacitors M_{23} and M_{25}. At the high frequency, the equivalent g_{m2} is reduced when g_{m3} increased. Therefore, the degradation of p_1 as a function of g_{m3} is power-efficiently attenuated by the proposed technique without changing the DC-gain.

According to the simulation, the proposed method can save 10% the total power of the amplifier compared to the conventional design at large values of g_{m3}. Fig. 10 shows the simulation results for equivalent MOSFET resistances of $M_{21} \sim M_{22}$ and the transconductance adjustment factor A, as a function of the output load current amplitude. It indicates that the control sensitivity of the factor A at $I_{\text{load}} = 0.1$ mA is about 0.35/decade.

D. Class-G Mode

The proposed chip also supports the feature of dynamic power supply conditioning (Class-G mode), where the supply voltage can automatically switch between +/−0.9 V and +/−1.8 V. Fig. 11 shows the block diagram of the Class-G

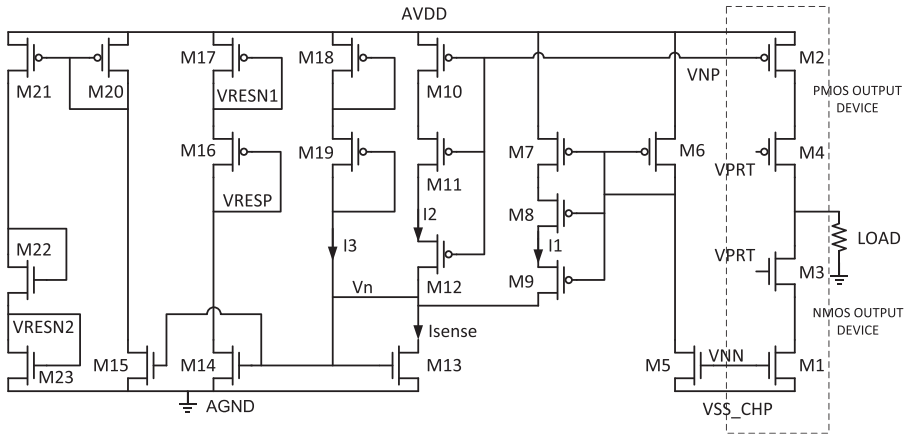


Fig. 9. Proposed current sensing circuit schematic, where transistors $M_1 \sim M_4$ are the same as transistors $M_{17} \sim M_{20}$ in Fig. 6.

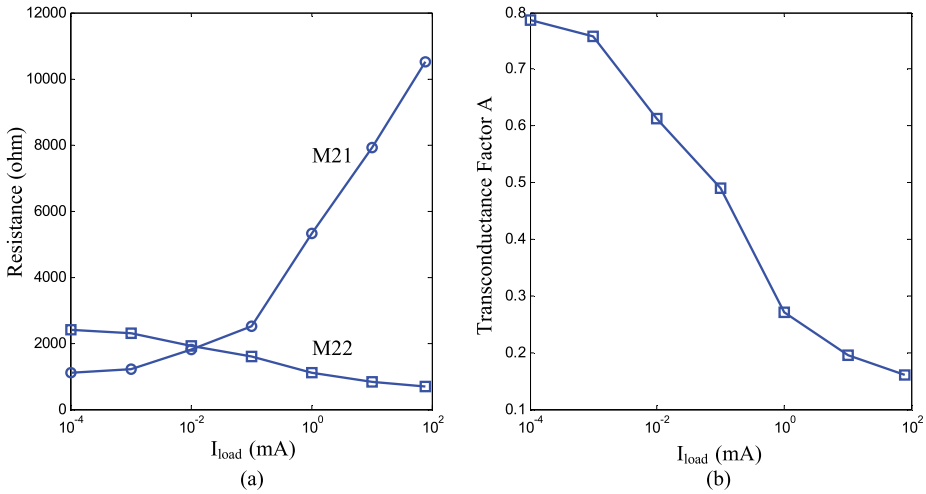


Fig. 10. The simulation results for (a) equivalent MOSFET resistances of $M_{21} \sim M_{22}$ and (b) the transconductance compensation factor A, as a function of the output load current amplitude.

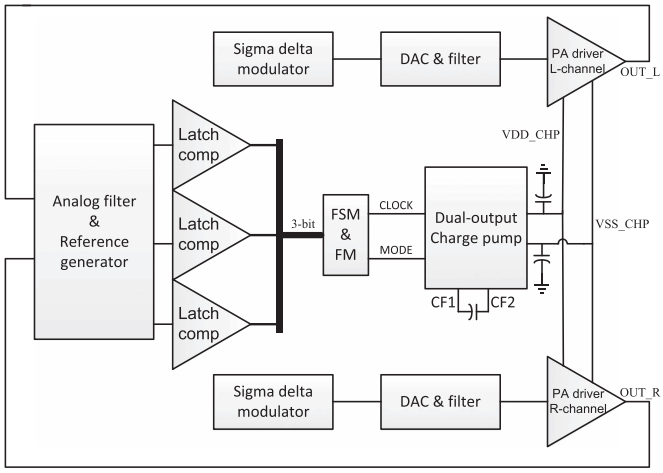


Fig. 11. Block diagram of the dynamic supply conditioning.

scheme. The power amplifier output is firstly low-pass filtered to attenuate the out-audio-band high frequency noise and then quantized by three hysteresis comparators which form a 2-bit flash A/D converter. The reference voltage for each hysteresis comparator can also be adjusted by programming the on-chip registers through the peripheral I^2C or I^2S communication interface. The quantized digital code is further processed in the digital logic block to create the control signals for the adaptive power supply conditioning. Moreover, efforts are made to guarantee the low switching distortion during the operation mode change. Supply voltage is changed with a limited slew rate, which can reduce the directly coupled switching noise in the output voltage. Limited slew rate of the supply voltage in the output stage will not significantly increase the harmonic distortion, since the high open-loop gain of the first two stages can attenuate the impact due to supply voltage variation of the third stage. In order to save the switching power, phase modulator and clock frequency modulator are also adopted to avoid frequently switching the charge pump operating mode.

IV. Measurement Results

The proposed chip is designed and fabricated using CMOS 55 nm process and Fig. 12 shows the designed chip layout with partitioning of main blocks. The designed input signal amplitude range is from -110 dBV to 0 dBV. The threshold

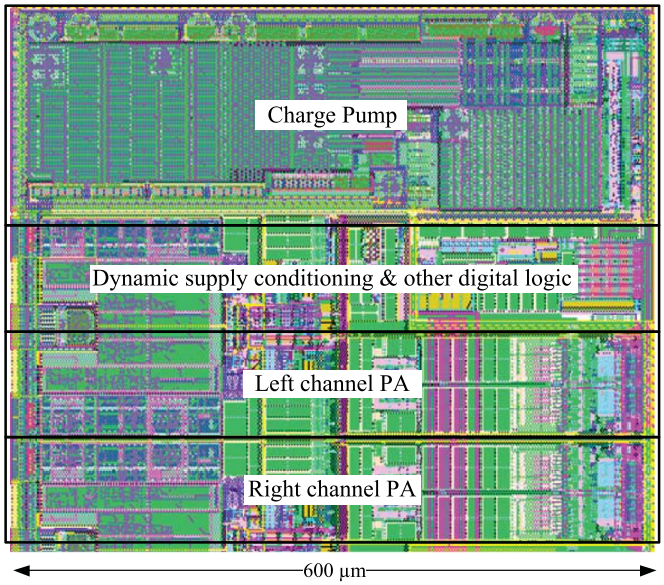


Fig. 12. Layout of the fabricated chip.

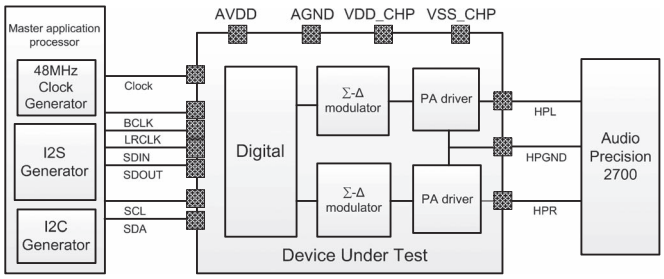


Fig. 13. Chip test environment setup.

voltage used for Class-G mode to switch the supply voltage is 550 mV. The switching frequency of the charge pump can be set from 1 MHz to 10 MHz. The charge pump is located at the top of the chip. The bottom half of the chip is the left/right audio channels and other analog circuits, while the digital circuit is mainly placed in the middle with noise isolation guardring. Fig. 13 illustrates the chip testing platform including the master application processor, device under test (DUT) and audio signal performance test equipment AP2700 [20]. The master application processor generates all the control logics and clocks as well as I2S and I2 C bus signals. The DUT as a slave device processes the input data to drive the test equipment AP2700. The static current consumption of the core chip is 350 μA with a 16 ohm resistive load, in which the PA, the charge pump and the rest control modules consumes 250 μA, 80 μA and 20 μA, respectively. The achieved output power is 55 mW for 1% THD+N [22].

Fig. 14 indicates the waveform of the measured A-weighted THD+N versus input signal amplitude. Input signal frequency is 1 KHz and the noise bandwidth is from 20 Hz to 20 KHz. The number of harmonics is 20 and the capacitive load is 1 nF. For Class-AB mode, the entire audio driver achieves 106 dB A-weighted dynamic range under 16 ohm load with a close-loop gain range from -6 dB to 6 dB. When operating under dynamic supply conditioning mode, the dynamic range can

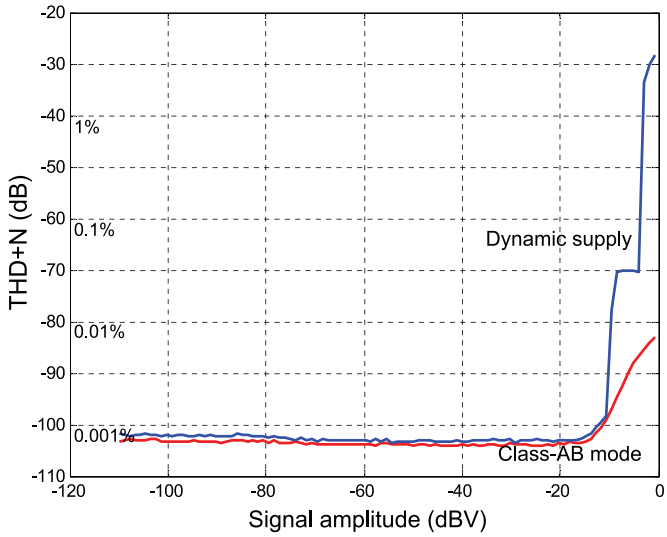


Fig. 14. Measured A-weighted THD+N versus input signal amplitude with 1 KHz signal frequency, 0 dB gain, 20 Hz to 20 KHz noise band, 20 harmonics and 1 nF capacitive load.

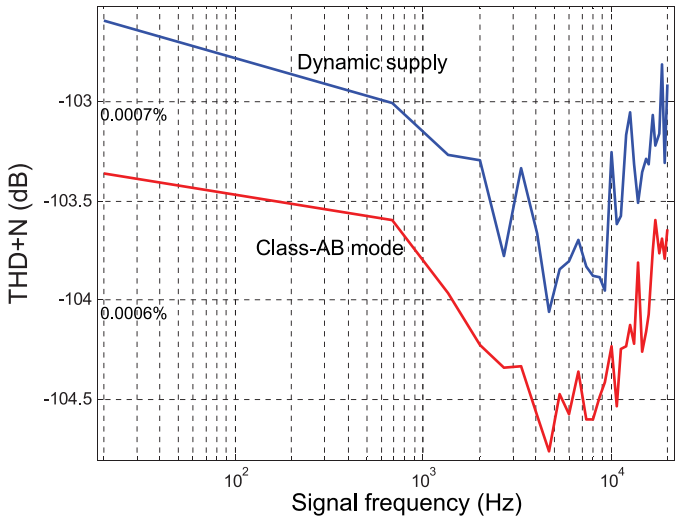


Fig. 15. Measured A-weighted THD+N versus input signal frequency with -60 dBV signal amplitude, 0 dB gain, 20 Hz to 20 KHz noise band, 20 harmonics and 1 nF capacitive load.

still achieve better than 104 dB. It is clear that, when larger than -15 dBV, the signal amplitude can significantly affect the linearity and Class-AB performs much better than dynamic supply conditioning for a very large signal amplitude.

Fig. 15 shows the waveform of THD+N versus input signal frequency under -60 dBV input signal amplitude with similar test conditions as Fig. 14, which proves that the dynamic range is almost constant in the whole audio band from 20 Hz to 20 KHz. Fig. 16 shows the measurement result of THD+N under different load capacitance of 5 pF, 1 nF and 20 nF for Class-AB mode. For less than -15 dBV signal amplitude, the THD+N is hardly affected by the load capacitance and both normal Class-AB and dynamic supply conditioning feature have very stable performance.

The FFT measurement result for Class-AB and dynamic supply conditioning modes are depicted in Fig. 17 with

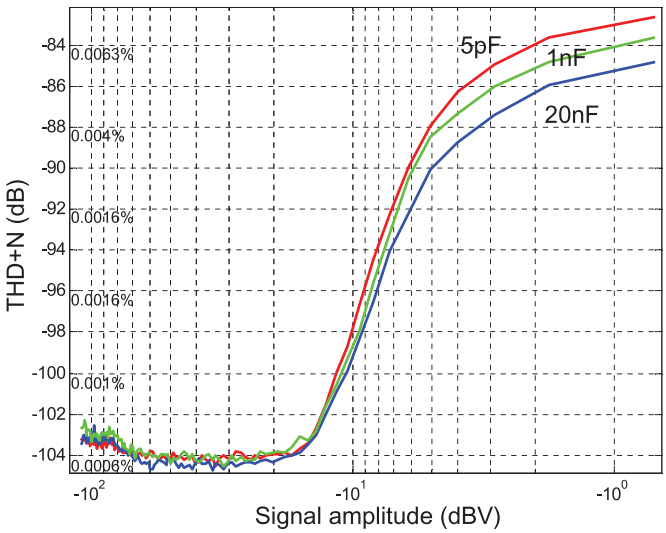


Fig. 16. Measured A-weighted THD+N versus input signal amplitude in Class-AB mode, under different load capacitances, 5 pF, 1 nF, 20 nF with 1 KHz signal frequency, 0 dB gain, 20 Hz to 20 KHz noise band, 20 harmonics and 16 ohm resistive load.

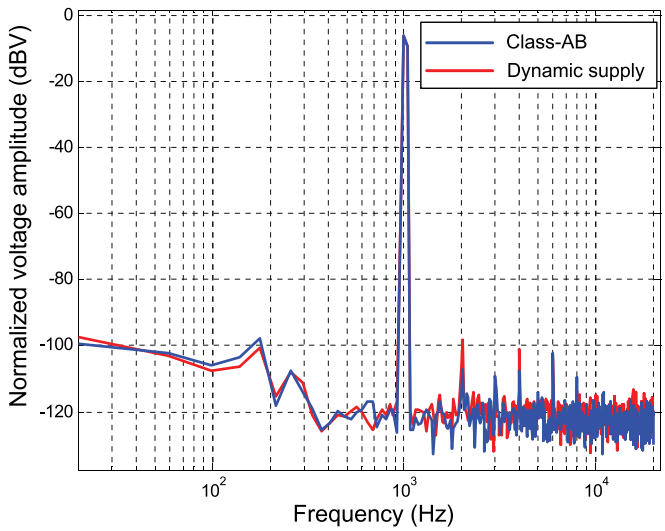


Fig. 17. Measured FFT for Class-AB and dynamic supply conditioning modes with 8192 sampling points with 0 dB gain, 1 nF and 16 ohm load.

8192 sampling points, which shows similar noise floors in both two modes. Supply conditioning introduces a little bit higher noise floor because the switching noise of the charge pump is incompletely attenuated by the loop gain. Moreover, the second order harmonic distortion is only about 9 dB less than that of the third order due to the adopted pseudo-differential architecture [21].

The measurement result of click-pop noise is illustrated in Fig. 18. The noise within the audio band from 300 Hz to 20 KHz shows less than −75 dBV. Fig. 19 is the transient measurement result of the dynamic supply conditioning PA with 1 KHz sinusoid output. The power supply VDD_CHIP and VSS_CHIP are switched when the signal is at the threshold points about +/−0.5 V. Neither obvious spike nor nonlinear distortion is superposed in the output waveform during the power supply transition between +/−1.8 V and +/−0.9 V. Table I summarizes

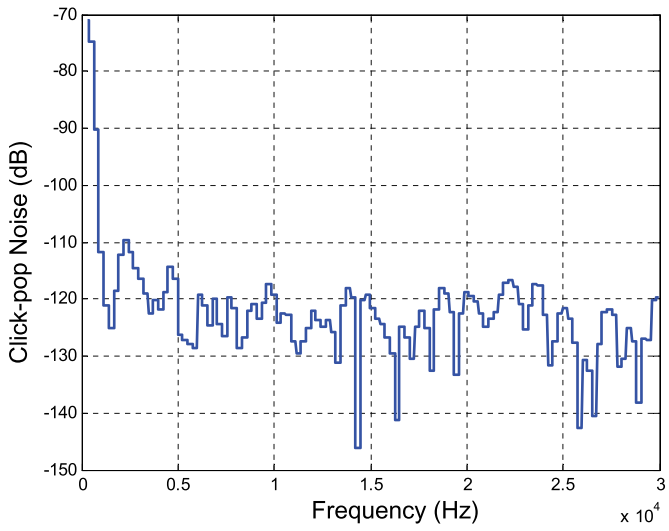


Fig. 18. Measured result of the click-pop noise power spectrum density.

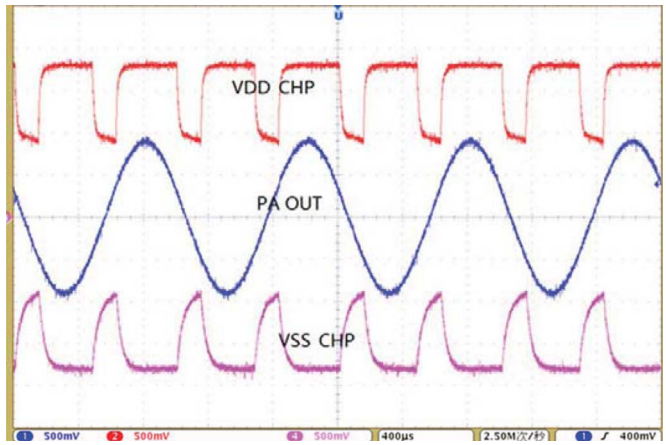


Fig. 19. Transient measurement result of the dynamic supply conditioning mode.

the measurement results of this work and compares it with the state-of-the-art designs, showing that the proposed PA with dynamic transconductance compensation technique provides −85 dB THD+N, 106 dB signal dynamic range with only 0.6 mA static current consumption.

V. Conclusion

This paper presents a low power Class-AB power amplifier using CMOS 55 nm process. By introducing a dynamic transconductance compensation technique, the bandwidth of the amplifier can be extended when a light loading is presented. The proposed technique is also valid for the dynamic supply conditioning (Class-G) mode operating with a single flying capacitor charge pump. The proposed power amplifier core circuit consumes only 0.35 mA static current and can provide 55 mW maximum output power and −85 dB THD+N, which shows state-of-the-art power efficiency and performance.

TABLE I
SUMMARY OF MEASUREMENT RESULTS AND COMPARISON

Specifications	2014[1]	2006 [2]	2009 [4]	2012 [6]	2013 [7]	2012 [12]	This work
CMOS Process	40 nm	350 nm	130 nm	180 nm	180 nm	500 nm	55 nm
Load capacitance	-	0~300 pF	1pF~22 nF	-	-	10 pF~5 nF	5 pF~20 nF
Closed-loop gain	-	-	-	-	-	-4 V/V	-6dB~6dB
On-chip charge pump and DAC	Yes/Yes	No/Yes	No/No	-	No/No	-	Yes/Yes
Supply voltage	4.5 V	0.8 V	1.2 V /2.0 V	2.65 V ~ 4.5 V	4.5 V	3 V	1.8 +/- 0.2 V
Core static current	-	-	-	-	-	-	0.35 mA[1] (with charge pump)
Total static current	0.84 mA	3 mA	1 mA	1.15 mA	0.6 mA	1.43 mW	0.6 mA
Output power	82 mW	28 mW	40 mW	60 mW	62 mW	93.8 mW	55 mW
Dynamic range	100dB	88dB	92dB	111dB	108dB	-	106dB[2]
THD+N	-84dB	-69dB	-84dB	-95dB	-88dB	-77.9 dB	-85dB[3]
FOM	21.69	11.67	33.33	19.68	22.96	65.5	50.93[4]

[1] 10% power saving due to the proposed dynamic transconductance compensation scheme

[2] With 1KHz signal, 20Hz ~20KHz noise band, 0dB gain, 20 harmonics, 1 nF & 16 ohm load

[3] With 1KHz, -60dBV signal, 20Hz~20KHz noise band, 0dB gain, 20 harmonics, 1 nF & 16 ohm load

[4] FOM = Output power/(Supply voltage × Total static current)

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